HAMZA OBEIDI

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EDUCATION

Bachelor of Applied Science in Nanotechnology Engineering, University of Waterloo 2025–2030

Relevant Coursework: NE 140 Linear Circuits, NE 111 Python Fundamentals

Engineering Society NE '30 Representative; Nanotechnology Academic Representative

EXPERIENCE

Isotope Laboratory Research Assistant May 2026 – Sept 2026

University of Waterloo *Waterloo, ON*

- Operated, calibrated, and troubleshot a gas chromatograph and mass spectrometer at one of the largest isotope labs in North America, diagnosing faults through systematic root-cause analysis.
- Prepared and analyzed 100+ environmental DIC and DOC samples in a clean-room environment, applying structured quality checks to ensure data integrity across the analytical pipeline.

Bio-mechatronics Systems Design Oct 2025 – Current

University of Waterloo Biotron *Waterloo, ON*

- Defined system architecture, requirements, and software-hardware interfaces across sensors, actuators, and embedded control, driving CAD development from specification through working prototype.
- Authored design specifications and interface documentation to guide firmware integration and component selection, enabling reliable iteration across a cross-functional team.

Quality Assurance Analyst Oct 2023 – Jan 2024

TAMVOES Health *Kitchener, ON*

- Designed and executed 30+ test cases against defined backend requirements, identifying and documenting 6 reproducible bugs to improve production reliability.
- Communicated structured defect reports to cross-functional developers, contributing to iterative release cycles and systematic pipeline improvements.

PROJECTS

EMG-Controlled Robotic Hand (Embedded Firmware, AD8221, DSP, CI, Verilog)

- Built a 5-channel EMG acquisition circuit (AD8221, ~100x gain) and Arduino firmware sampling at 500 Hz to process forearm muscle signals into proportional PWM control of 5 servo actuators.
- Building a CI-tested DSP pipeline to validate the rectify to smooth to threshold signal chain, and reimplementing core processing stages in Verilog RTL for FPGA simulation (in progress).

RV32I Pipelined CPU Core (SystemVerilog, cocotb, Verilator, OpenLane 2, SKY130)

- Designed a 5-stage, 47-instruction RV32I pipeline in SystemVerilog with data forwarding, hazard detection, and a 2-bit branch predictor; verified with cocotb and Verilator passing the official riscv-tests suite and a Python ISA reference model comparing every register write.
- Synthesized and laid out on SKY130 via OpenLane 2 with closed timing; added SymbiYosys formal verification, CI on every push, and CPI and predictor analysis from RISC-V GCC benchmarks.

Fab Root-Cause Assistant (Python, SQL, Machine Learning, SHAP, Streamlit)

- Built an end-to-end ML pipeline on the UCI SECOM semiconductor dataset (1,567 production runs, 590 sensor features) — cleaning data in SQL, applying SPC with Western Electric rules to isolate a July-August process excursion, and training an imbalanced failure classifier.
- Validated a weekly-retraining strategy that caught October failures a static model missed; built per-run SHAP explanations and a Streamlit dashboard for engineer-facing root-cause investigation.

SKILLS

Programming	Python (NumPy, Pandas, SciPy, scikit-learn), C, C++, Java, MATLAB, SQL (SQLite), SystemVerilog / Verilog
Software	REST APIs, LLM Integration, CI/CD, Git, Machine Learning, SHAP, SPC, Streamlit, Embedded Firmware
Systems	Microcontrollers (Arduino, ESP32), DSP, Analog Circuit Design, PCB Design (KiCad), SolidWorks